AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 32, line 2 as follows:

A method, system, and computer program product are disclosed for managing data in a cache. A first cache memory is provided that includes data. A second cache memory is provided that also includes data in which at least some of the data in the first cache memory is the same as at least some of the data in the second cache memory. In response to a request for data that is stored in both the first and second cache memories, one of the cache memories ~~are~~ is chosen in accordance with an access balancing technique. The access balancing technique may include[[:]] at least one of selection using round robin, and selection based on statistical analysis such as access frequency of the first and second cache memories. First and second access balancing techniques may be used for data accessed from the cache memories, which may comprise disk data and control data, such as data indicating whether data in the caches has been modified and is write pending.

Please amend the paragraph beginning on page 9, line 10 as follows:

Each of the slots represents data that is read from the disk storage area 42 and stored in one or both of the cache memories 22, 24. The control data for each of the slots indicates the state of the data in the slot. Thus, for example, the control data element for a slot can indicate that the data has been read from the disk storage area 42 but not written to by the host 44 (i.e., not modified by the host 44). Alternatively, the control data element for a slot could indicate that the data in the slot has been written to by the host 44 since being read from the disk storage area 42 (i.e., write pending). Note that, generally, data that is read from the disk storage area 42 but

not subsequently modified may be eliminated from the cache without any ultimate loss of data since the data in the cache memories 22, 24 is the same as the data in the disk storage area 42. On the other hand, data that is write pending (i.e., modified while in the cache memories 22, 24 after being read from the disk storage area 42) is written back to the disk storage area 42 for proper data synchronization. Note also that the control data could indicate that the associated slot contains data that is the same in both of the cache memories 22, 24, which could occur, for example, either when the data is write pending or immediately after data that is write pending is written to the disk.

Please amend the paragraph beginning at page 19, line 7 as follows:

The partial flow chart 80a of Fig. 9 illustrates an alternative step 82' that corresponds to the step 82 of Fig. 6 where the control data is accessed. As discussed above, for embodiments illustrated herein, the control data is the same for both of the cache memories 22, 24. The step 82' represents choosing which of the cache memories 22, 24 to use for accessing the control data based on a statistical analysis. Although many different types of statistical analysis techniques could be used and would be apparent to one of ordinary skill in the art, for one embodiment of the invention, the statistical analysis of Fig. 82' simply tallies the number of accesses of each of the memories 22, 24 over a predetermined amount of time, such as one second. That is, if for the one second prior to the current access, the number of accesses of the cache memory 22 is N and the number of accesses to the cache memory 24 is M, then, if $N < M$, the cache memory 22 will be used, since the cache memory 22 is the one of the cache memories 22, 24 having the least number of previous accesses in the previous one second. Steps ~~associate~~ associated with the connector A' shown in Figure 9 are described in more detail elsewhere herein.

Please amend the paragraph beginning at page 21, line 19 as follows:

Referring to Fig. 14, a diagram illustrates specialized hardware 152 for providing the functionality, or at least a portion of the functionality, described above in connection with Figs. 9-13. The hardware 152 may be implemented using any one of a variety of technologies for designing customized hardware. The hardware 152 may be implemented using a single chip or a plurality of chips. The hardware 152 may receive access requests for a cache via one or both of the buses 26, 28, or through some means (not ~~shown~~ illustrated in Fig. 14) The hardware 152 may then process the requests in accordance with one or more of the techniques discussed above, and then read the data from one of the cache memories 22, 24.

Please amend the paragraph beginning at page 22, line 5 as follows:

Note that using the hardware 152 may reduce the requirements of keeping additional statistics because the hardware may have direct access to ~~a queue length and other~~ information used in connection with the techniques described herein.

Please add the following as a new paragraph at page 22 following the paragraph on page 22, lines 5-7:

In accordance with one aspect of the invention is a computer program product for managing data in a cache. Machine executable code is included for: providing a first cache memory that contains data; providing a second cache memory that contains data wherein at least some of the data in the first cache memory is the same as at least some of the data in the second

cache memory; and, in response to a request for data that is stored in both the first cache memory and the second cache memory, choosing one of the cache memories to use to obtain the data according to an access balancing technique.